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2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/486,779	Applicant(s) HUANG, ALEX Q.	
	Examiner Steven Loke	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,19-38 and 42-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-9,22-37 and 42-44* is/are rejected.

7)☒ Claim(s) *1,19-21 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *12 March 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The disclosure is objected to because of the following informalities: Fig. 3A discloses reference numeral [74] is pointing to an N-type region. However, the specification shows reference numeral [74] is a P base (page 9, line 18).

Appropriate correction is required.

2. Claims 1-9, 19-21, 23-38 and 42-44 are objected to because of the following informalities:

Claim 1, lines 8-9, the phrase "metal oxide semiconductor transistor (MOS)" is unclear. The phrase should rewrite as "metal oxide semiconductor (MOS) transistor".

Claim 1, line 10, "and" should change to "and".

Claim 1, line 17, "[said] a" should change to "a".

Claims 2-9, line 1, the phrase "An emitter controlled thyristor device" is unclear whether it is being referred to "An emitter controlled thyristor device package" of claim 1.

Claim 4, line 4, the phrase "thyristor emitter" is unclear whether it is being referred to "said thyristor emitter".

Claim 9, line 2, the phrase "MOS" is unclear whether it is being referred to "MOS transistor".

Claim 19, line 29, the phrase "[emitter controlled]" should be deleted.

Claim 20, lines 3-4, the phrase "said first, second and third metal layers" has no antecedent basis.

Claim 23, line 15, the phrase "[MOS]" should be deleted.

Claim 23, lines 8-9, the phrase "said MOS transistors" has no antecedent basis.

Claim 31, lines 7-8, the phrase "said thyristor gate terminal" has no antecedent basis.

Claim 32, line 4, the phrase "said gate terminal" has no antecedent basis.

Claim 33, lines 15-17, the phrase "means for shorting said emitter of said thyristor element to a terminal of said first discrete semiconductor switch or for injecting electrons..." is unclear. It should rewrite as "means for shorting said emitter of said thyristor element to a terminal of said first discrete semiconductor switch for injecting electrons...".

Claim 33, lines 22-23, the phrase "said first discrete electronic switch" and line 25, the phrase "said first electronic switch" have no antecedent basis.

Claim 33, lines 6-7, the phrase "said thyristor device" has no antecedent basis.

Claims 34-36, line 2, the phrase "said thyristor device" has no antecedent basis.

Claims 34-38, line 1, the phrase "An emitter turn-off thyristor" is unclear whether it is being referred to "An emitter turn-off thyristor device package" of claim 33.

Claim 42, lines 3-4, the phrase "MOS transistor" is unclear whether it is being referred to "a MOS transistor".

Appropriate correction is required.

3. Claims 4-9, 32, 43 and 44 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification only discloses an emitter turn-off thyristor package with a GTO thyristor and first and second MOS transistors in figs. 17A-17D. The specification never discloses a third MOS transistor for the package as claimed in claim 4.

The specification only discloses an emitter turn-off thyristor package with a GTO thyristor, an NMOS transistor and a PMOS transistor in figs. 17A-17D. The specification never discloses the first MOS transistor comprises a PMOS transistor for the package as claimed in claim 5.

The specification only discloses an emitter turn-off thyristor package with a GTO thyristor, an NMOS transistor and a PMOS transistor in figs. 17A-17D. The specification never discloses the first MOS transistor comprises a PMOS transistor and a third MOS transistor comprises an NMOS transistor for the package as claimed in claim 6.

The specification only discloses an emitter turn-off thyristor package with a GTO thyristor, an NMOS transistor and a PMOS transistor in figs. 17A-17D. The specification never discloses a third MOS transistor comprises an NMOS transistor for the package as claimed in claim 7.

The specification only discloses an emitter turn-off thyristor package with a GTO thyristor, an NMOS transistor and a PMOS transistor in figs. 17A-17D. The specification never discloses a diode connected between the gate of the first MOS transistor and the thyristor emitter for the package as claimed in claim 9.

The specification (page 22, lines 8-9 and amended fig. 18) discloses a capacitor [C600] connected in parallel to a MOS transistor Q2 (second switch). Amended fig. 19

also discloses a capacitor connected in parallel to a MOS transistor Q2 (second switch). However, the specification never discloses a capacitor connected in parallel to the MOS transistor of the first switching devices and connecting the second terminal of the MOS transistor of the first switching devices to the thyristor gate terminal as claimed in claim 32.

The specification (page 22, lines 10-12) discloses the gate switch Q2 (second switch) acts like a Zener diode. Original claim 29 also discloses the MOS switching devices comprise a diode. The specification never discloses the first discrete semiconductor switch includes a diode as claimed in claim 43. The specification also never discloses the first discrete semiconductor switch includes a zener diode as claimed in claim 44.

4. Claims 2, 3, 8, 22, 23-32 and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Since claim 1 discloses an emitter controlled thyristor device package comprising a thyristor, a first discrete MOS transistor and a second discrete MOS transistor, it is unclear how a floating ohmic contact of claim 2 can be formed in the package having the first and second discrete MOS transistors and the thyristor. The floating ohmic contact can only be formed in the integrated form of the device as shown in fig. 1A.

Since claim 1 discloses an emitter controlled thyristor device package comprising a thyristor, a first discrete MOS transistor and a second discrete MOS transistor, it is unclear how a metal strap of claims 3 and 8 can be formed in the package having the

first and second discrete MOS transistors and the thyristor. The metal strap can only be formed in the integrated form of the device as shown in fig. 1A.

Since claim 39 has been canceled, it is unclear why claim 22 is still depend to claim 39.

Claim 23, lines 8-9, the phrase "a first terminal of said MOS transistors" is unclear whether it is being referred to "a first terminal of each of said first plurality of discrete switching devices"; lines 9-10, the phrase "a second terminal of said MOS transistors" is unclear whether it is being referred to "a second terminal of each of said first plurality of discrete switching devices"; lines 14-15, the phrase "a first terminal of said switching devices" is unclear whether it is being referred to "a first terminal of each of said second plurality of switching devices"; lines 15-16, the phrase "a second terminal of said switching devices" is unclear whether it is being referred to "a second terminal of each of said second plurality of switching devices"; lines 19-20, the phrase "a gate terminal of said first plurality of switching devices" is unclear whether it is being referred to "a gate terminal of each of said first plurality of switching devices"; lines 23-24, the phrase "said gate of said first plurality of switching devices" is unclear whether it is being referred to "said gate terminal of each of said first plurality of switching devices".

Claim 24, lines 6-7, the phrase "said switching devices" is unclear whether it is being referred to the first or the second switching devices.

Since claim 25 discloses a third metal plate, it is unclear where are the first and second metal plates in claims 25.

Claims 26-30, lines 2-3, the phrase "said switching devices" is unclear whether it is being referred to the first or the second switching devices.

Claim 31, lines 4, 7, the phrase "said MOS transistors" is unclear whether it is being referred to "each of said first plurality of switching devices".

Claim 32, lines 2-3, the phrase "said first switching devices comprise a MOS transistor" is unclear whether it is being referred to "each of said first switching devices comprises a MOS transistor".

Since claim 33 discloses an emitter turn-off thyristor device package including a thyristor element, a first discrete semiconductor switch and a second discrete semiconductor switch, it is unclear how the thyristor element and at least one of the first and second semiconductor switches are formed monolithically as claimed in claim 34.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 33, 35-37 and 42-44 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Broich et al.

In regards to claim 33, Broich et al. show all the elements of the claimed invention in figs. 4 and 6 and col. 5, line 45 to col. 6, line 33 of the specification. It is a thyristor device package, including a GTO thyristor element [2'] having an anode terminal [9], an emitter terminal [5] (it is well known in the art that the cathode terminal (emitter terminal) [5] of a GTO thyristor is connected to the emitter region of a GTO thyristor) and a gate

terminal [8'], a first discrete semiconductor switch [1] connected in series with the emitter terminal [5] of the thyristor [2'] element by a first terminal [3] of the first semiconductor switch, a second discrete semiconductor switch [25] connected in series with the gate terminal [8'] of the thyristor device by a first terminal of the second discrete semiconductor switch; second terminals (6, a terminal of the Zener diode [25]) of the first and second discrete semiconductor switches being connected together, and means (connecting line [4]) for shorting the emitter of the thyristor element to a terminal [3] of the first discrete semiconductor switch for injecting electrons into the thyristor for triggering the thyristor into a latching state when the MOS transistor [1] is in an on-state (col. 6, lines 10-21); wherein the first and second discrete semiconductor switches are arranged such that a signal of a first type applied to the first discrete semiconductor switch [1] turns the thyristor to an on-state and a signal of a second type applied to the first discrete semiconductor switch turns the thyristor to an off-state (col. 6, lines 10-21).

Since the currents are entered into the thyristor via the emitter region of the thyristor and the first switch is connected to the emitter region, the thyristor [2'] is considered as an emitter turn-off thyristor.

In regards to claim 35, Broich et al. further disclose the thyristor [2'] and the first and second semiconductor switches [1, 25] are formed as discrete devices.

In regards to claim 36, Broich et al. further disclose the thyristor and the first and second semiconductor switches are commonly packaged.

In regards to claim 37, Broich et al. further disclose the first semiconductor switch [1] is an MOS device.

In regards to claim 42, Broich et al. further disclose the first discrete semiconductor switch [1] includes a MOS transistor.

In regards to claim 43, Broich et al. further disclose the second discrete semiconductor switch [25] includes a diode.

In regards to claim 44, Broich et al. further disclose the second discrete semiconductor switch [25] includes a zener diode.

7. Applicant's arguments with respect to claims 32, 33, 34, 37 and 42 have been considered but are moot in view of the new ground(s) of rejection.

8. Claims 1, 19 and 23 would be allowable if rewritten or amended to overcome the objections set forth in this Office action.

9. Claim 23 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

10. Claim 38 would be allowable if rewritten to overcome the objection set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: The first major difference in the claims not found in the prior art of record is an emitter controlled thyristor comprising a thyristor, a first discrete MOS transistor and a second discrete MOS transistor. The thyristor device is easily controlled even in a high current conduction state and the discrete components of the device package are able to control a high current operation of the thyristor. The second major difference in the claims not found in the prior art of record is the a thyristor device package comprising: a

thyristor, a first discrete MOS transistor and a second discrete MOS transistor; and the thyristor and first and second transistors formed between the first and second metal plates. The thyristor formed between the metal plates can dissipate heat more quickly. The third major difference in the claims not found in the prior art of record is a thyristor device package comprising: a thyristor, a first plurality of discrete switching devices and a second plurality of discrete switching devices. The fourth major difference in the claims not found in the prior art of record is at least one of the first and second semiconductor switches is constituted by a plurality of semiconductor devices. The device package having a plurality of first or second switches is able to reduce the parasitic inductance in the current path between the anode and cathode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
May 18, 2003

Steven Loke
Primary Examiner